### LAMBDA ADVANCED ANALOG INC. 🖄

PRELIMINARY

# AHV2800 Series

Hybrid - High Reliability DC/DC Converters

### DESCRIPTION

The AHV series of DC/DC converters are designed to replace the AHE/ATO family of converters in applications requiring compliance to MIL-STD-704A through E, in particular the input surge requirement of 80 volts specified in MIL-STD-704A. The converters are designed to withstand transient input voltage of 80 volts. No input voltage or output power derating is necessary over the full military temperature range.

These converters are packaged in an extremely rugged, low profile package that meets all requirements of MIL-STD-883 and MIL-PRF-38534. Parallel seam weld sealing and the use of ceramic pin feedthru seals assure long term hermeticity after exposure to extended temperature cycling.

The basic circuit is a push-pull forward topology using power MOSFET switches. The nominal switching frequency is 500 KHz. A unique current injection circuit assures current balancing in the power switches. All AHV series converters use a single stage LC input filter to attenuate input ripple current. A low power 11.5 volt series regulator provides power to an epitaxial CMOS custom pulse width modulator integrated circuit. This single integrated circuit provides all PWM primary circuit functions. Power is transferred from primary to secondary through a ferrite core power transformer. An error voltage signal is generated by comparing a highly stable reference voltage with the converter output voltage and drives the PWM through a unique wideband magnetic feedback circuit. This proprietary feedback circuit provides an extremely wide bandwidth, high gain control loop, with high phase margin. The feedback control loop gain is insensitive to temperature, radiation, aging, and variations in manufacturing. The transfer function of the feedback circuit is a function of the feedback transformer turns ratio which cannot change when subjected to enviromental extremes.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are available in four screening grades to satisfy a wide range of requirements. The CH grade is fully compliant to the requirements of MIL-PRF-38534 for class H. The HB grade is processed and screened to the class H requirement, but may not necessarily meet all of the other MIL-PRF-38534 requirements, e.g., element evaluation and Periodic Inspection (P.I.) not required. Both grades are tested to meet the complete group "A" test specification over the full military temperature range without output power deration. Two grades with more limited screening are also available for use in less demanding applications. Variations in electrical, mechanical and screening can be accommodated. Contact Lambda Advanced Analog for special requirements.

#### **FEATURES**

- 80 Transient (100 msec max.) Absolute Maximum Input
- 50 V<sub>DC</sub> Absolute Maximum Input (Continuous)
- 16-40 V<sub>DC</sub> Input Range
- Single, Dual, and Triple Outputs
- 15 Watt Output Power (No Temperature Derating)
- Low Input/Output Noise
- Full Military Temperature Range
- Wideband PWM Control Loop
- Magnetic Feedback
- Low Profile Hermetic Package (.405")
- Short Circuit and Overload Protection
- Constant Switching Frequency (500 KHz)
- True Hermetic Package (Parallel Seam Welded, Ceramic Pin Feedthru

### SPECIFICATIONS (SINGLE OUTPUT MODELS)

TCASE = -55°C to +125°C, VIN = +28 V ±5% unless otherwise specified

### ABSOLUTE MAXIMUM RATINGS

Input Voltage Power Output Soldering **Temperature Range**  -0.5 V to 50 VDC (Continuous) 80 V (100ms) Internally limited, 17.5W typical 300°C for 10 seconds (1 pin at a time) -55°C to 135°C case<sup>9</sup> Operating Storage -65°C to +135°C

		Conditions								
		-55°C - Tc - +125°C, VIN = 28 VDC	Group A	AHV	2805S	AHV	2812S	AHV	2815S	
TestSymbol ±5%, CL=0,	unless otherw	rise specified Subgroups	Min	Max	Min	Max	Min	Max	Units	
STATIC CHARACTER	ISTICS									
OUTPUT Voltage Current Ripple Voltage <sup>1</sup>	Vout Iout Vrip	VIN = 16, 28, and 40 VDC IOUT = 0 VIN = 16, 28, and 40 VDC VIN = 16, 28, and 40 VDC BW = DC to 1 MHz	1 2,3 1,2,3 1,2,3	4.95 4.90 0.0	5.05 5.10 3.00 60	11.88 11.76 0.0	12.12 12.24 1.25 60	14.85 14.70 0.0	15.15 15.30 1.00 60	V V A mV p-p
Power	Ρουτ	$V_{IN} = 16, 28, and 40 V_{DC}$	1,2,3	15		15		15		W
REGULATION Line Load	VRLINE VRLOAD	VIN = 16, 28, and 40 VDC IOUT = 0, Half Load and Full Load VIN = 16, 28, and 40 VDC IOUT = 0, Half Load and Full Load	1,2,3		5 25 50		30 60 120		35 75 150	mV mV mV
INPUT										
Current	lin	IOUT = 0, Inhibit (pin 2) = 0 IOUT = 0, Inhibit (pin 2) = Open	1,2,3		18 50		18 50		18 50	mA mA
Ripple Current		IOUT = Full Load	1,2,3		50		50		50	mA p-p
EFFICIENCY	EFF	Io∪⊤ = Full Load Tc = +25°C	1	72		72		72		%
ISOLATION	ISO	Input to output or any pin to case (except pin 8) at 500 VDC, Tc = +25°C	1	100		100		100		MΩ
CAPACITIVE LOAD 2,3	CL	No effect on DC performance Tc = +25°C	4		500		200		200	μF
LOAD FAULT POWER DISSIPATION	PD	Overload, Tc = +25°C <sup>4</sup> Short circuit, Tc = +25°C	1		8.5 8.5		8.5 8.5		8.5 8.5	W W
SWITCHING FREQUENCY	Fs	Io∪⊤ = Full Load	4	450	550	450	550	450	550	KHz
DYNAMIC CHARACT	ERISTIC	S								
STEP LOAD CHANGES Output Transient <sup>5</sup> Recovery <sup>5,6</sup>	VOTLOAD TTLOAD	No Load 135 50% 50% Load 135 100% Load No Load 335 50% Load	4 4 4 4	-300 -500	+300 +500 70 200 5	-300 -750	+300 +750 70 1500 5	-300 -750	+300 +750 70 1500	mVpk mVpk μS μS
		50% Load 335 No Load	4		5		C		5	ms
STEP LINE CHANGES Output Transient Recovery	VOTLINE TTLINE	Input step 16 to 40 VDC <sup>3,7</sup> Input step 40 to 16 VDC <sup>3,7</sup> Input step 16 to 40 VDC <sup>3,6,7</sup> Input step 40 to 16 VDC <sup>3,6,7</sup>	4 4 4		300 -1000 800 800		500 -1500 800 800		500 -1500 800 800	mVpk mVpk μS μS
TURN-ON Overshoot Delay	VTON OS TON D	IOUT = OA and Full Load IOUT = O and Full Load <sup>8</sup>	4,5,6 4,5,6		550 10		750 10		750 10	mVpk ms
LOAD FAULT RECOVERY	trLF	VIN = 16 TO 40 VDC	4,5,6		10		10		10	ms

Notes:

Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz. 1.

Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability 2. but will interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.

3.

Parameter shall be guaranteed to the limits specified. An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power 4. dissipation.

5

Load step transition time between 2 and 10 microseconds. Recovery time is measured from the initiation of the transient to where Vout has returned to within ±1 percent of Vout at 50 percent load. 6.

7 Input step transition time between 2 and 10 microseconds.

Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the 8. input.

9. Above 125°C case temperature, derate output power linearly to 0 at 135°C case.

### SPECIFICATIONS (DUAL OUTPUT MODELS)

TCASE = -55°C to +125 °C, VIN = +28 V ±5% unless otherwise specified

### ABSOLUTE MAXIMUM RATINGS

Input Voltage Power Output Soldering Temperature Range -0.5 V to 50 VDC (Continuous) 80 V (100ms) Internally limited, 17.5W typical 300°C for 10 seconds (1 pin at a time) Operating -55°C to 135°C case <sup>13</sup> Storage -65°C to +135°C

		Conditions						
		-55°C - Tc - +125°C, VIN = 28 VDC	Group A	AHV2			2815D	
Test	Symbol	±5%, CL=0, unless otherwise specified	Subgroups	Min	Max	Min	Max	Units
STATIC CHARACTERISTICS								
OUTPUT Voltage <sup>1</sup>	Vout	IOUT = 0	1 2,3	±11.88 ±11.76	±12.12 ±12.24	±14.85 ±14.70	±15.15 ±15.30	VV
Current <sup>1,2</sup> Ripple Voltage <sup>1,3</sup>	Iout Vrip	VIN = 16, 28, and 40 VDC VIN = 16, 28, and 40 VDC BW = DC TO 2 MHZ	1,2,3 1,2,3	0.0	±625 60	0.0	±500 60	mA mV p-p
Power <sup>1,2,4</sup>	POUT	$V_{IN} = 16, 28, and 40 V_{DC}$	1,2,3	15		15		W
REGULATION			, , -	_		-		
Line <sup>1,5</sup>	VRLINE	VIN = 16, 28, and 40 VDC	1		30		35	mV
Load <sup>1</sup>	IOUT VRLOAD	IOUT = 0, Half Load and Full Load VIN = 16, 28, and 40 VDC IOUT = 0, Half Load and Full Load	2,3 1,2,3		60 120		75 150	mV mV
INPUT								
Current	lin	Io∪⊤ = 0, inhibit (pin 2) Tied to input return (pin 10)	1,2,3		18		18	mA
Ripple Current <sup>3</sup>	IRIP	IOUT = 0, inhibit (pin 2) = open IOUT = Full Load BW = DC to 2MHz	1,2,3		65 50		65 50	mA mA p-p
EFFICIENCY	Eff	louτ = FULL LOAD, Tc = +25°C	1	72		72		%
ISOLATION	ISO	Input to output or any pin to case (except pin 8) at 500 VDc, Tc = +25°C	1	100		100		MΩ
CAPACITIVE LOAD 6,7	CL	No effect on DC performance, TC = $+25^{\circ}$ C	4		200		200	μf
LOAD FAULT POWER DISSIPATION PD		Over Load, Tc = +25°C <sup>8</sup> Short Circuit, Tc = +25°C	1		8.5 8.5		8.5 8.5	W W
SWITCHING FREQUENCY	Fs	IOUT = FULL LOAD	4	450	550	450	550	KHz
DYNAMIC CHARACTERI	STICS							
STEP LOAD CHANGES								
Output Transient 9	VOTLOAD	50% Load 135 100% Load No Load 135 50% Load	4	-300 -500	+300 +500	-300 -500	+300 +500	mVpk mVpk
Recovery 9,10	TTLOAD	50% Load 135 100% Load	4	-500	+500	-500	70	μs
·····		No Load 335 50% Load 50% Load 335 No Load	4		1500 5		1500 5	µs ms
STEP LINE CHANGES								
Output Transient 7,11	VOTLINE	Input step 16 to 40 VDC Input step 40 to 16 VDC	4		1200 -1500		1500 -1500	mVpk
Recovery 7,10,11	TTLINE	Input step 40 to 16 VDC Input step 16 to 40 VDC Input step 40 to 16 VDC	4 4 4		-1500 4 4		-1500 4 4	mVpk ms ms
TURN-ON	1							-
Overshoot <sup>1</sup> Delay <sup>1,12</sup>	Overshoot <sup>1</sup> VTON OS IOUT = O an		4,5,6 4,5,6		600 10		600 10	mVpk ms
LOAD FAULT RECOVERY	<sup>7</sup> trLF		4,5,6		10		10	ms

Notes:

1. Tested at each output

2. Parameter guaranteed by line and load regulation tests.

3. Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.

4. Total power at both outputs.

5. When operating with unbalanced loads, at least 25% of the load must be on the positive output to maintain regulation.

 Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.

7. Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified.

8. An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.

9. Load step transition time between 2 and 10 microseconds.

10. Recovery time is measured from the initiation of the transient to where VouT has returned to within ± 1 percent of VouT at 50 percent load.

11. Input step transition time between 2 and 10 microseconds.

12. Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.

13. Above 125°C case temperature, derate output power linearly to 0 at 135°C case.

### **SPECIFICATIONS (TRIPLE OUTPUT MODELS)** TCASE = $-55^{\circ}$ C to $+125^{\circ}$ C, VIN = +28 V $\pm 5\%$ unless otherwise specified

### ABSOLUTE MAXIMUM RATINGS

Input Voltage Power Output Soldering Temperature Range -0.5 V to 50 VDC (Continuous) 80 V (100ms) Internally limited, 17.5W typical 300°C for 10 seconds (1 pin at a time) Operating -55°C to 135°C case <sup>8</sup> Storage -65°C to +135°C

		Conditions -55°C - Tc - +125°C, VIN = 28 VDC	Group A	AHV2	2812T	AHV	2815T	
Test	Symbol	$\pm 5\%$ , CL=0, unless otherwise specified	Subgroups	Min	Max	Min	Max	Unit
STATIC CHARACTERISTI	CS							
OUTPUT Voltage 1	Vout	IOUT = 0 (main)	1 2,3	4.95 4.90	5.05 5.10	4.95 4.90	5.05 5.10	V V
		IOUT = 0 (dual) <sup>1</sup>	2,3 1 2,3	±11.88 ±11.76	±12.12 ±12.24	±14.85 ±14.70	±15.15 ±15.30	V V V
Current <sup>1,2,3</sup>	Ιουτ	VIN = 16, 28, and 40 VDC (main) VIN = 16, 28, and 40 VDC (dual) <sup>1</sup>	1,2,3 1,2,3	0.0	2000 ±208	0.0	2000 ±167	mA mA
Ripple Voltage <sup>1,4</sup>	Vrip	VIN = 16, 28, and 40 VDC BW = DC TO 2 MHz (main)	1,2,3		80		80	mV p-p
Power <sup>1,2,3</sup>	Роит	VIN = 16, 28, and 40 VDC BW = DC TO 2 MHz (main) VIN = 16, 28, and 40 VDC (main) (+dual) (-dual) (total)	1,2,3 1,2,3 1,2,3 1,2,3 1,2,3 1,2,3	10 2.5 2.5 15	40	10 2.5 2.5 15	40	mV p-p W W W
REGULATION			1,2,0			10		
Line <sup>1,3</sup>	VRLINE	VIN = 16, 28, and 40 VDC IOUT = 0, 1000, 2000 mA (main)	1,2,3		25		25	mV
		$V_{IN} = 16, 28, and 40 V_{DC}$ $I_{OUT} = 0, \pm 104, \pm 208 mA (\pm 12V) (dual)$	1		±30		±35	mV
Load <sup>1,3</sup>	VRLOAD	IOUT = 0, ±84, ±167 mA (±15v) VIN = 16, 28, and 40 VDC IOUT = 0, 1000, 2000 mA (main)	2,3 1,2,3		±60 50		±75 50	mV mV
		VIN = 16, 28, and 40 VDC $IOUT = 0, \pm 104, \pm 208 mA (\pm 12V) (dual)$ $IOUT = 0, \pm 84, \pm 167 mA (\pm 15v)$	1,2,3		±60		±75	mV
INPUT								
Current	lin	IOUT = 0 inhibit (pin 8) tied to input return (pin 10) IOUT = 0	1,2,3 1,2,3		15 50		15 50	mA mA
Ripple Current <sup>4</sup>	IRIP	inhibit (pin 2) = open lout = 2000 mA (main) lout = $\pm 208$ mA ( $\pm 12V$ ) lout = $\pm 167$ mA ( $\pm 15V$ ) BW = DC to 2MHz	1,2,3		50		50	mA p-p
EFFICIENCY	EFF	IOUT = 2000  mA (main) $IOUT = \pm 208 \text{ mA (}\pm 12\text{V})$ $IOUT = \pm 167 \text{ mA (}\pm 15\text{V})$	1	72		72		%
ISOLATION	ISO	Input to output or any pin to case (except pin 7) at 500 Vdc, Tc = +25C	1	100		100		MΩ
LOAD FAULT POWER DISSIPATION <sup>3</sup>	PD	Over Load, Tc = +25C⁵ Short Circuit, Tc = +25C	1		8.5 8.5		8.5 8.5	W W
SWITCHING FREQUENCY <sup>1</sup>	Fs	IOUT = 2000  mA (main) $IOUT = \pm 208 \text{ mA (}\pm 12V)$ $IOUT = \pm 167 \text{ mA (}\pm 15V)$	4	450	550	450	550	KHz
CAPACITIVE LOAD 6,7	CL	No effect on DC performance, Tc = +25C (main) (dual)	4		500 200		500 200	µf µf
DYNAMIC CHARACTERIS	STICS							
STEP LOAD CHANGES Output Transient <sup>9</sup>	VOTLOAD	50% Load 135 100% Load	4	-300	+300	-300	+300	mVpk
Recovery 9,10	TTLOAD	No Load 135 50% Load 50% Load 135 100% Load No Load 335 50% Load 50% Load 335 No Load	4 4 4 4	-400	+400 100 2000 5	-400	+400 100 2000 5	mVpk µs µs ms

STEP LINE CHANGES Output Transient <sup>7,11</sup> Recovery <sup>7,10,11</sup>	VOTLINE TTLINE	Input step 16 to 40 VDC Input step 40 to 16 VDC Input step 16 to 40 VDC Input step 40 to 16 VDC	4 4 4 4	1200 -1500 4 4	1200 -1500 4 4	mVpk mVpk ms ms
TURN-ON Overshoot <sup>1</sup> Delay <sup>1,12</sup>	VTon os Ton d	IOUT = 0 and $\pm 625$ mA IOUT = 0 and $\pm 625$ mA	4 4	750 15	750 15	mVpk ms
LOAD FAULT RECOVERY 7	trLF		4	15	15	ms

Notes:

Tested at each output

2. Parameter guaranteed by line and load regulation tests.

3. At least 25 percent of the total power should be taken from the (+5 volt) main output.

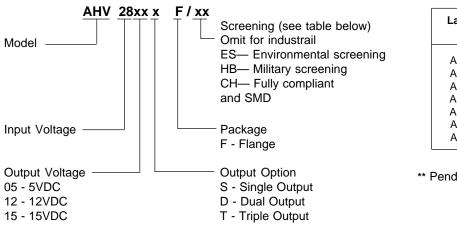
- 4. Bandwidth guaranteed by design. Tested for 20 KHz to 2 MHz.
- An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.

6. Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.

Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified.
Above 125°C case temperature, derate output power linearly to 0 at 135°C case.

- 9. Load step transition time between 2 and 10 microseconds.
- 10. Recovery time is measured from the initiation of the transient to where VOUT has returned to within ± 1 percent of VOUT at 50 percent load.
- 11. Input step transition time between 2 and 10 microseconds.
- 12. Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 8) while power is applied to the input.

### PART NUMBER



## STANDARD MILITARY DRAWING CROSS REFERENCE

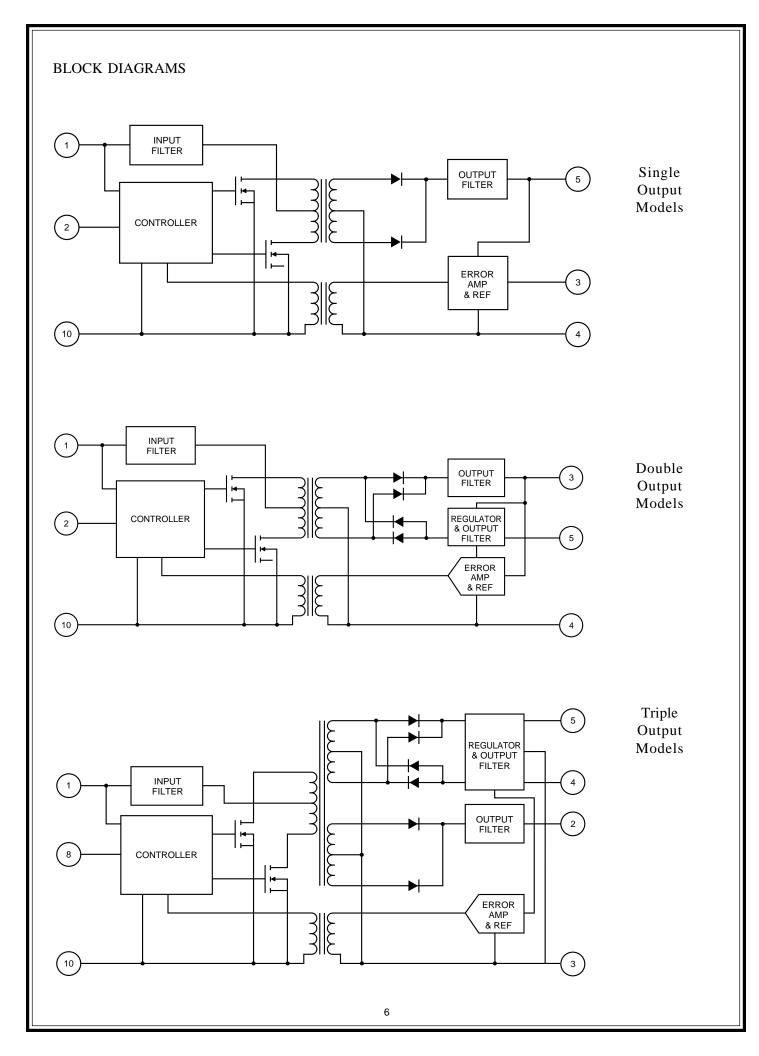
Standardized ** military dwg.
5962-91773
5962-92112
5962-92113
5962-92114
5962-92774
5962-92115
5962-92116

\*\* Pending consult factory for status.

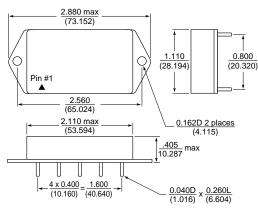
### SCREENING DETAILS

Requirement	MIL-STD-883 Method	No Suffix	ES Suffix	HB Suffix	CH Suffix
Temperature Range		-20°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Element Evaluation					MIL-PRF-38534
Internal Visual	2017	12	1	1	1
Temperature Cycle	1010		Cond B	Cond C	Cond C
Constant Acceleration	2001		500g	Cond A	Cond A
Burn-in	1015		96 hrs @125°C	160 hrs @125°C	160 hrs @125°C
Final Electrical (Group A)	MIL-STD-38534 & Specification	25°C	25°C	-55, +25, +125°C -	55, +25, +125°C
Seal, Fine & Gross	1014	Cond A	Cond A, C	Cond A, C	Cond A, C
External Visual	2009	15	1	1	1

per Commercial Standards

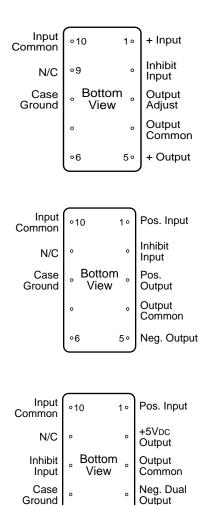


### MECHANICAL OUTLINE



Single and Dual Output Models

### PIN DESIGNATION



N/C

۰6

Pos. Dual

Output

5°

### Single Output Models

2.700 max (68.580)

2.360 (59.944)

1.950 (49.530)

 $\frac{4 \times 0.400}{(10.160)} = \frac{1.600}{(40.640)}$ 

Flange

**Triple Output Models** 

Pin #1

Pin 1 Positive Input Pin 2 Inhibit Input Pin 3 Output adjust\* Pin 4 Output common Pin 5 Positive output Pin 10 Input common Pin 9 N/C Pin 8 Case gnd Pin 7 N/C Pin 6 N/C

1.345

(34.163)

0.410 max. 10.414

0.162D 2 places (4.115)

0.040D (1.016) x 0.260L (6.604) 1.00

(25.400)

### **Dual Output Models**

Pin 1 Positive Input Pin 2 Inhibit Input Pin 3 Positive output Pin 4 Output common Pin 5 Negative output Pin 10 Input common Pin 9 N/C Pin 8 Case gnd Pin 7 N/C Pin 6 N/C

### **Triple Output Models**

Pin 1 Positive Input Pin 2 +5Vbc output Pin 3 Output common Pin 4 Neg. Dual output (12/15Vbc) Pin 5 Pos. Dual output (12/15Vbc)

Pin 7 Case gnd Pin 6 N/C

Pin 8 Inhibit Input

Pin 9 N/C

Pin 10 Input common

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### APPLICATION INFORMATION

#### Inhibit function

Connecting the inhibit pin (Pin 2 of single and dual models, pin 8 of triple models) to the input return (Pin 10) will cause the converter to shut down and operate in a low power standby mode. Power consumption in this mode is calculated by multiplying Vin times the input current inhibited, typically 225mw at Vin equal to 28 volts. The input current inhibited is relatively constant with changes in Vin. The open circuit inhibit pin voltage is typically 11.5 volts and can be conveniently driven by an open collector driver. An internal pullup resistor enables the user to leave this pin floating if the inhibit function is not used in their particular application. All models use identical inhibit internal circuits. Forcing inhibit pin to any voltage between 0 and 6 volts will assure the converter is inhibited. The input current to this pin is  $500\mu a$  maximum at Vpin2 = to 0 volts. The converter can be turned on by opening Pin 2 or forcing a voltage from 10 to 50 volts. Inhibit pin current from 10 to 50 volts is less than  $\pm 50\mu a$ .

### EMI Filter

An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461 CEO3

\*Output Adjust (Single Output Models Only)

The output voltage of the AHV28XXS can be adjusted upward by connecting Output Adjust (Pin 3) and Output Common (Pin 4) as shown in Table 1.

Resistance, ohm	Output Voltage Increase, %					
Pin 3 to 4	5V	12V	15V			
Х	0	0	0			
390 K	+1.0 %	+1.6%	+1.7 %			
145 K	+2.0 %	+3.2 %	+3.4 %			
63 K	+3.1 %	+4.9 %	+5.1 %			
22 K	+4.1 %	+6.5 %	+6.8 %			
0	+5.0 %	+7.9 %	+8.3 %			

Table 1: Output Adjustment Resistor Values

<sup>©</sup>Lambda Advanced Analog

The information in this data sheet has been carefully checked and is believed to be accurate; however no responsibility is assumed for possible errors. These specifications are subject to change without notice.

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